Research Article

Negative Capacitance Effect at the Interface Between Si Wafers with Undulating Surfaces

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The field emission current in a vacuum ($I_T = \alpha E^2/e^{\beta/E}$, where α and β are constants) depends on the electric field strength E. In other words, the differential resistance $(dI_T/dV)^{-1}$ in a vacuum does not follow Ohm's law. Therefore, the relationship governing the capacitance and current between two electrodes in a vacuum is an intriguing research topic. In this study, we construct an interface structure in which contact areas and non-contact vacuum areas coexist by adhering two Si wafers and measure the capacitance characteristics of this structure. A volatile capacitance appears at the interface, with the contact areas contributing to positive capacitance and the vacuum areas contributing to negative capacitance. The tunneling current passing through the interface plays an important role in the formation of the negative capacitance.

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Recently, research concerning negative capacitance has attracted considerable interest[1][2][3]. In these studies, the negative capacitance is related to the physical properties of the dielectric material between the electrodes. Unlike the negative capacitance due to material properties, our research group proposed a two-resistor structure model and generated negative capacitance by controlling the tunneling current across the interface of the two-resistor structure[4].

The equivalent circuit of a resistor R with two parallel-plate electrodes consists of the parallel circuit of R and the capacitor C. The capacitance C varies depending on the value of resistance R. If R is infinite, the capacitance C is determined by the dielectric constant of the insulator R. Moreover, when R depends on the potential difference V across the resistor, that is, when $dR/dV \neq 0$, the relationship between the electrode charge Q and V does not follow Ohm's proportional relationship.

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As Q leaks through the resistor R, the capacitance becomes volatile. Our theoretical study revealed that the volatile capacitance C is determined by the correlation between the differential current dV/dR and the Ohmic current V/R. The conclusions are that when $dV/dR > V/R$, $C < 0$; when $dV/dR = V/R$, $C = 0$; and when $dV/dR < V/R$, $C > 0$[4]. Furthermore, our experiments confirmed the transition between positive and negative capacitance in the interface structure of a multi-walled carbon nanotube resistor and vacuum, and the results obtained were consistent with theoretical predictions[4].

In this study, we investigate the volatile capacitance characteristics of a two-resistor structure constructed using Si crystals. Valuable results are obtained regarding the role of the tunneling current in the capacitance characteristics.

The p-type Si (100) wafers of thickness 520 μm and resistivity 10 Ω·cm have undulations on one side. Figures 1(a) and 1(b) show an SEM image of the surface and a cross-sectional schematic diagram of the undulating Si wafer, respectively. Figure 1(c) shows the pattern of the contact area between the undulating wafers, and Fig. 1(d) shows the pattern of the contact area between the undulating wafer and the untreated wafer. As shown in Figs. 1(a) and 1(b), the cross-section is an equilateral triangle with a distance of 4 μm between vertices. An aluminum thin film of thickness 100 nm is fabricated on one side of the Si wafer to form Ohmic contact, as shown in Fig. 1(b). The undulating surfaces of the two wafers face each other, set at 90° in the γ direction, to form sample A with point contact, as shown in Fig. 1(c). The contact points are assumed to be circular with a diameter of Φ_a. Additionally, sample B with line contact, as shown in Fig. 1(d), is formed by facing an undulating and a non-undulating wafer. The contact line width is assumed to be l_a. Samples A and B are square with a side length of 3 mm. A conceptual diagram of the two-resistor structure is shown in Fig. 2. The average distance between the two resistors is denoted by d. The current I passing through the interface is the sum of the conduction current I_E and the polarization current I_P through the contact areas and the tunneling current I_T through the non-contact vacuum areas. This interface, composed of contact and non-contact areas, forms the core of the negative capacitor structure. The average surface roughness of the Si wafers is 0.20 μm, and the interfacial electric field strength reaches 6.25 V/μm. The field emission threshold of p-type Si micro-tip arrays is 4.0-5.0 V/μm[5]. Therefore, it is feasible to generate the tunneling current passing through the interface of the two-Si wafer structure.

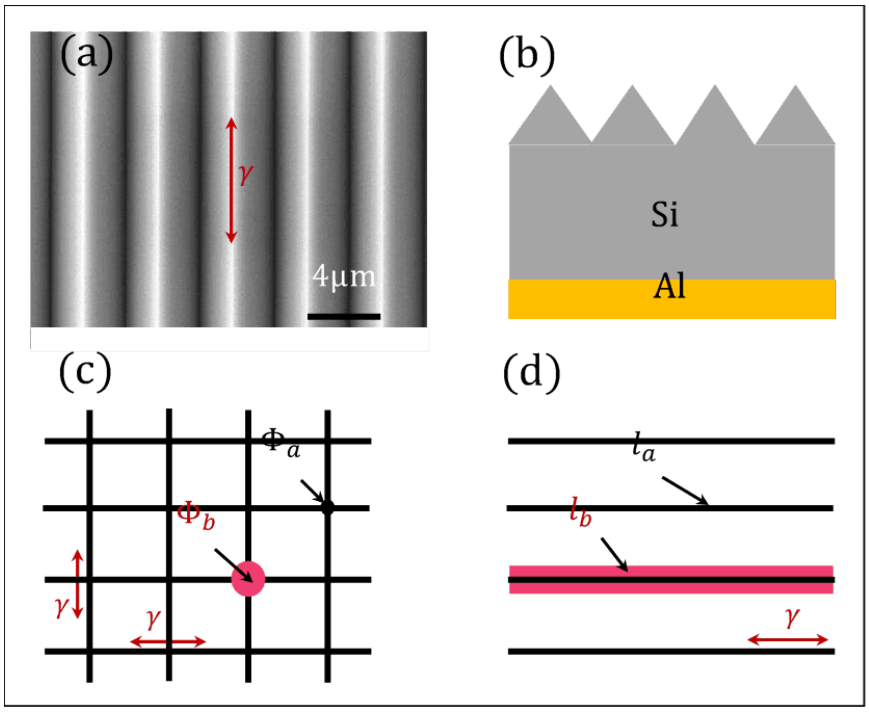

Figure 1. Surface SEM image (a) and cross-sectional schematic diagram of the undulating Si wafer, the pattern of contact area between the undulating wafers (c), and the pattern of contact area between the undulating wafer and the untreated wafer (d).

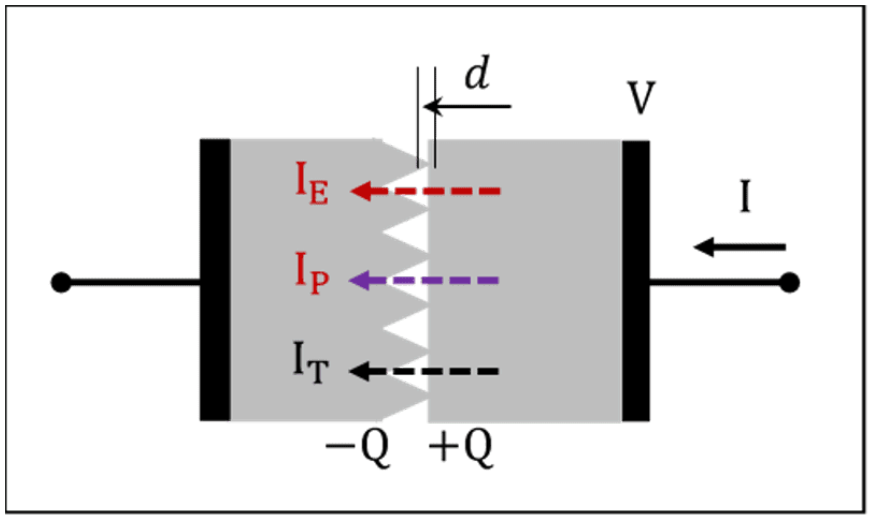

Figure 2. Conceptual diagram of the two-resistor structure.

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Samples A and B are placed in a vacuum chamber with a base vacuum of $2.0 \times 10^{-5} Pa$, and their electrical characteristics are measured with an impedance analyzer (HIOKI, IM3570) while varying the distance d, DC bias, and AC amplitude. To overcome the difficulty of controlling the distance d, it is adjusted using screws. The screw is rotated approximately 2° to change the distance d. A current source with constant I is applied during the measurements.

The frequency dependence of the capacitance for samples A and B at various d is shown in Figs. 3(a) and 3(b), respectively. The color bar in the figure indicates the number of measurements. For sample A, in the frequency range below $10^3\ Hz$, the capacitance changes from negative to positive and then back to negative with decreasing d, in the order of $10^{-8}\ F$. In the frequency range above $10^3\ Hz$, the capacitance remains almost constant at $3.5 \times 10^{-10}\ F$ at 1 MHz.

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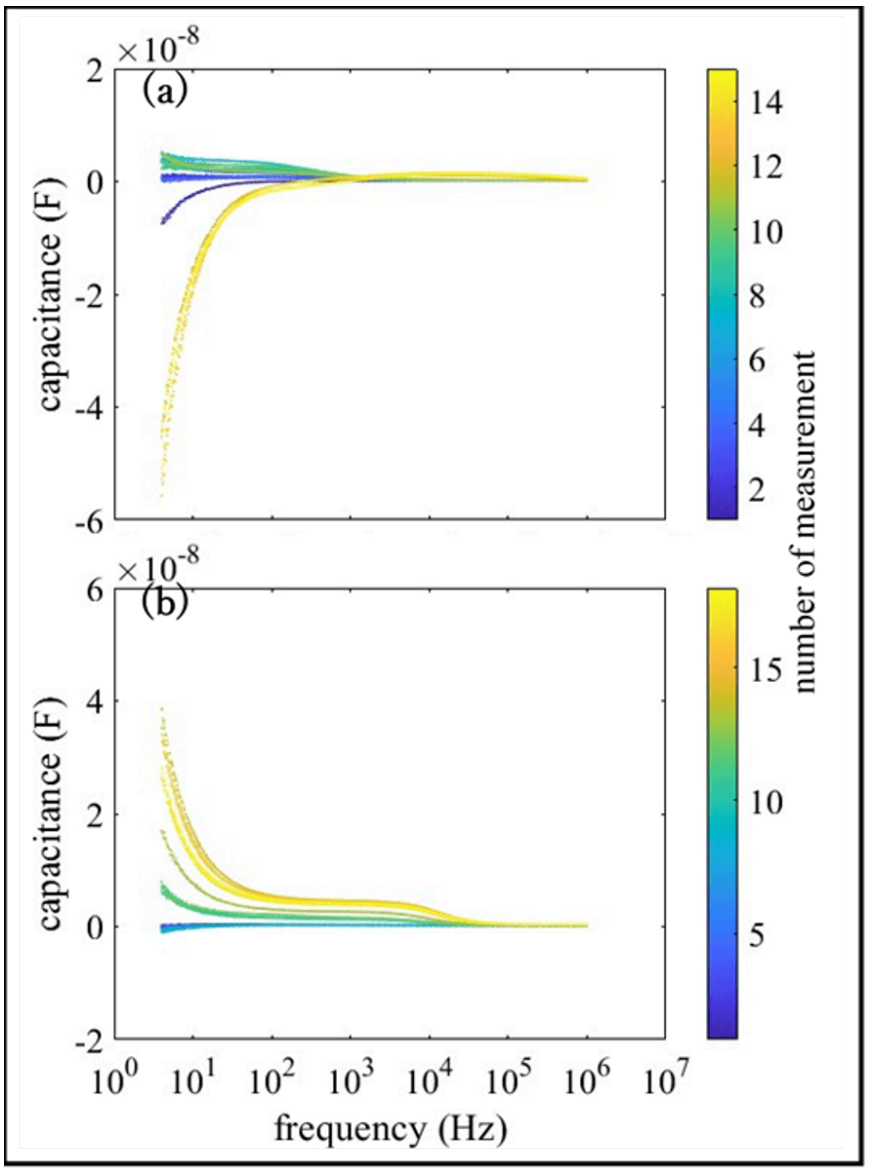

Figure 3. Frequency dependence of capacitance for samples A (a) and B (b) at various . The color bar in the figure indicates the number of measurements.

For sample B, negative capacitance appears in the frequency range below $10^2\ Hz$, increasing to positive with decreasing d, up to the order of $10^{-8}\ F$. Above $10^2\ Hz$, the capacitance remains almost constant at $2.5 \times 10^{-10}\ F$ at 1 MHz. These results suggest that the process of the two resistors approaching one another could be divided into two stages. In the first stage, with zero contact area between the two resistors, a tunneling current can occur if the resistors become sufficiently close. The initial negative capacitance with decreasing d can be attributed to the tunneling current. In the second

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stage, contact occurs between the two resistors, generating conduction and polarization currents in addition to the tunneling current, forming a positive capacitance component. A further reduction in the distance d between the two resistors changes the contact area and the proportion of tunneling current. As shown in Fig. 1, the contact area patterns of samples A and B are point and line, respectively. Assuming the diameter of the tunneling current point and the width of the tunneling current line to be Φ_b and l_b, respectively, the area ratio of the tunneling current can be estimated. For sample A, the ratio is $\alpha_A = S_T/S_{E+P} = \pi(\Phi_b/2)^2/\pi(\Phi_a/2)^2 = (\Phi_b/\Phi_a)^2$. For sample B, the ratio is $\alpha_B = s_t/s_{e+p} = l_b/l_a$. Assuming that $\Phi_a = l_a$ and $\Phi_b = l_b$, we obtain $\alpha_A/\alpha_B = (\Phi_b/\Phi_a)^2/(l_b/l_a) = \Phi_b/\Phi_a$, where $\Phi_b > \Phi_a$. In consideration of the resistance of the conduction and polarization currents, the proportion of tunneling current in sample A is greater than that in sample B. Thus, the smaller negative capacitance in sample B can be attributed to a smaller proportion of tunneling current. Assuming I_T decreases Q and I_E and I_P increase Q, the condition $dV/dR < V/R$ holds in sample B with the larger contact area, resulting in positive capacitance. This explains the results observed in Fig. 3.

The frequency dependence of the capacitance for samples A and B at various DC biases is shown in Figs. 4(a) and 4(b), respectively. Here, the AC amplitude is 2.5 V, d is set to its minimum value, and the color bar indicates the DC bias. The DC bias dependence of negative capacitance is strong in sample A, which has a large proportion of tunneling current. In contrast, in sample B, where the conduction and polarization currents are dominant, there is almost no DC bias dependence of capacitance. It is understood that the DC bias does not affect the differential current of the conduction and polarization currents $(dV/dR = V/R = constant)$, but does affect the differential resistance $(dI_T/dV)^{-1}$ corresponding to the tunneling current.

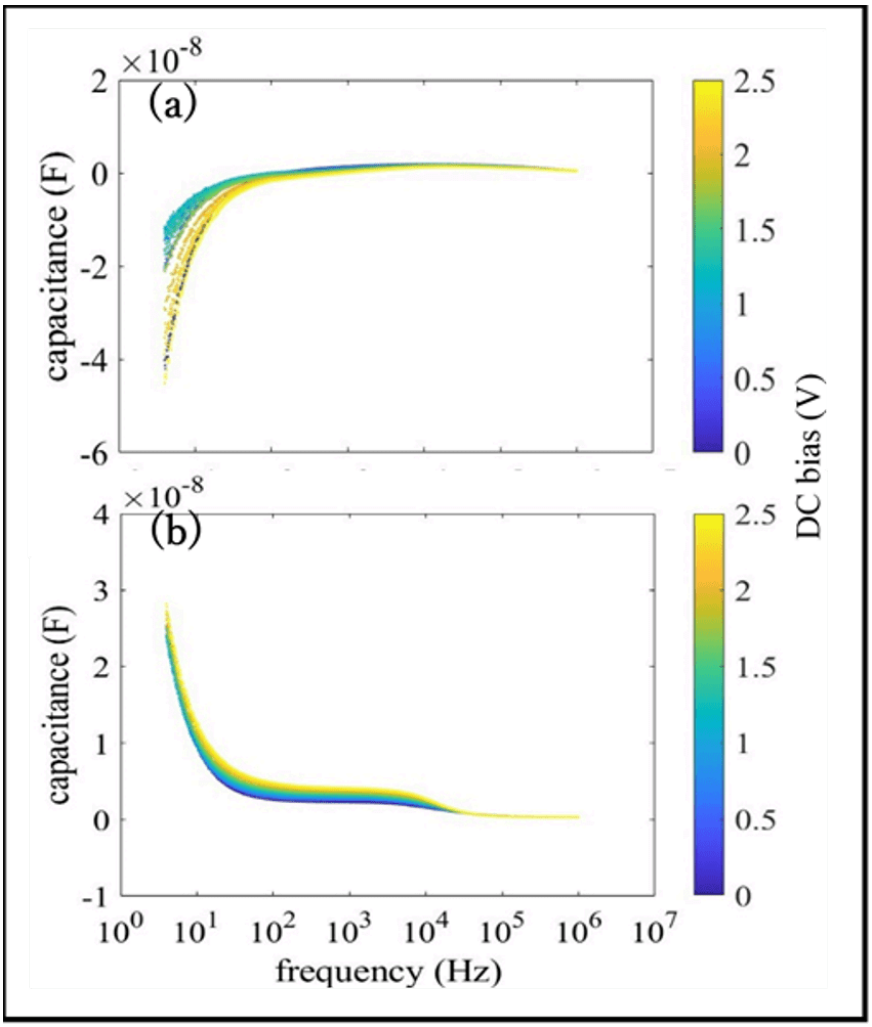

Figure 4. Frequency dependence of capacitance for samples A (a) and B (b) at various DC biases. Here, the AC amplitude is 2.5 V, is set to its minimum value, and the color bar indicates the DC bias.

The frequency dependence of the capacitance for samples A and B at various AC amplitudes is shown in Figs. 5(a) and 5(b), respectively. Here, the DC bias is 2.5 V, d is set to its minimum value, and the color bar indicates the AC amplitude. It is confirmed that the AC signal is periodic and does not affect the charge Q. This is similar to the characteristics of a dielectric capacitor[6].

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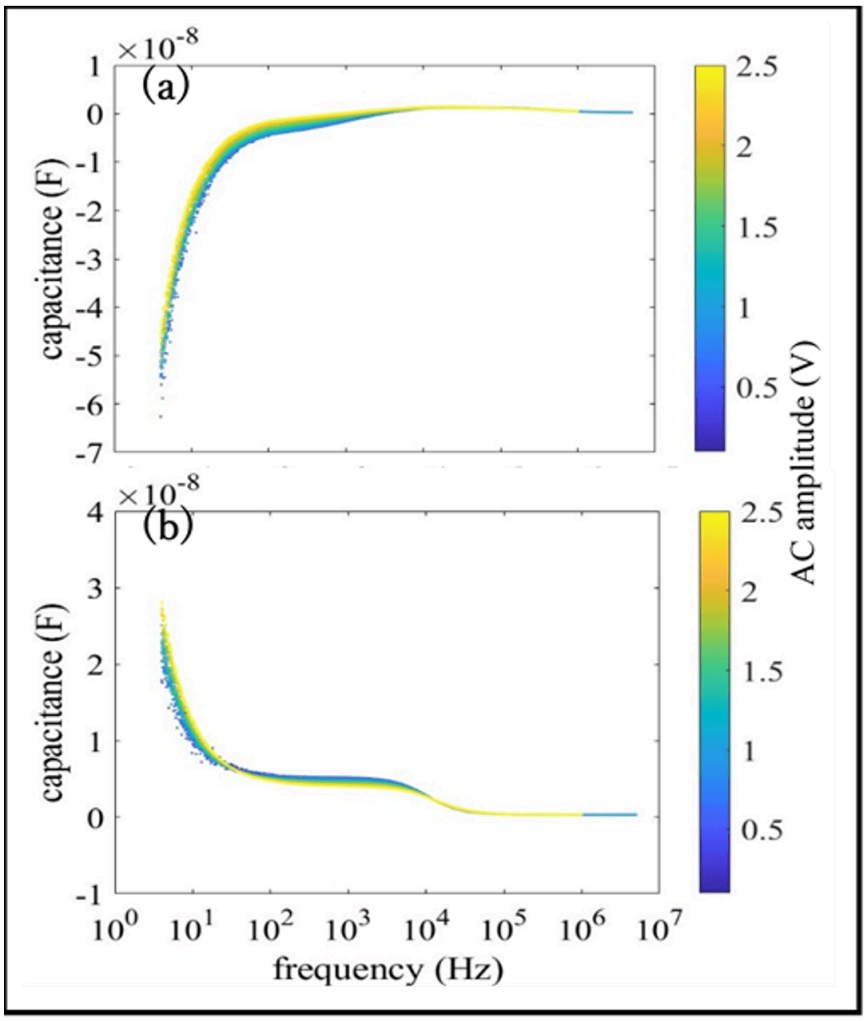

Figure 5. Frequency dependence of capacitance for samples A (a) and B (b) at various AC amplitudes. Here, the DC bias is 2.5 V, is set to its minimum value, and the color bar indicates the AC amplitude.

The results indicate that negative capacitance, i.e., inductance without a coil, may be achieved. Furthermore, it is confirmed that the phase delay of current relative to potential V is related to the time constant τ of an RC circuit. The frequency dependence of the time constant $\tau = R_s C_s$ for samples A and B at various d is shown in Figs. 6(a) and 6(b), respectively. Here, R_s and C_s represent the resistance and capacitance of the series equivalent circuit of the samples. Additionally, the straight lines in the figure indicate the half-periods of the AC signal. As can be observed by comparing Figs. 3 and 6, negative capacitance occurs in the low-frequency region where the half-periods of the AC signal are greater than τ. In other words, the relationship $\tau > half\ period$ must be established to form

negative capacitance. Under this condition, the tunneling current is sustained along with the AC signal. Conversely, when $\tau < half\ period$, the duration of sustained tunneling current during the AC signal is shorter, with periods where it reaches zero. In other words, the sustained tunneling current plays a crucial role in forming negative capacitance. Furthermore, peaks in the time constant can be observed in Figs. 6(a) and 6(b) under conditions where negative capacitance is generated. This can be attributed to the resonance between the negative capacitance (inductance) of the two-resistor structure and the positive capacitance of the Al electrodes[7].

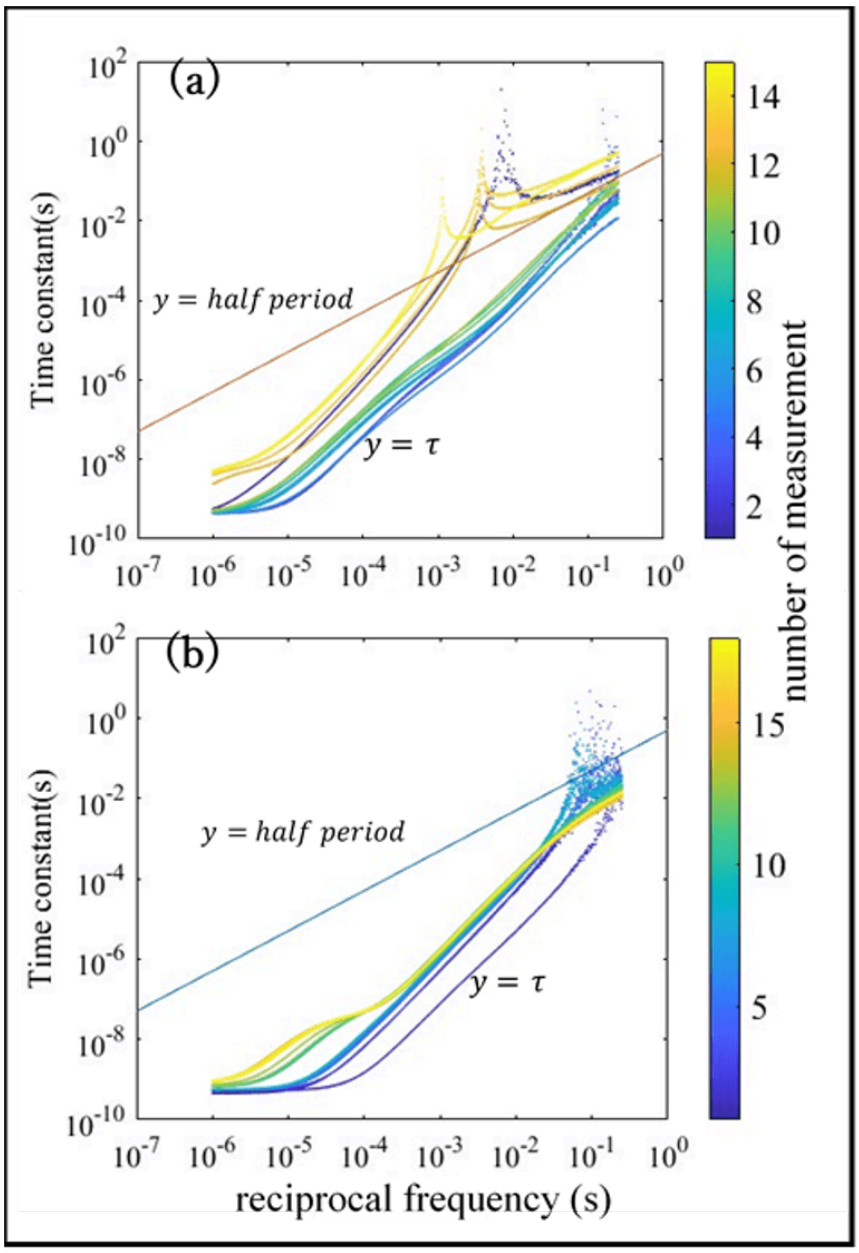

Figure 6. Frequency dependences of the time constant for samples A (a) and B (b) at various .

Figures 7(a) and 7(b) present the Cole–Cole plots for samples A and B at various d, respectively, with enlarged insets on the vertical axes. Corresponding to the results of Figs. 3 and 6, negative capacitance is observed in both samples A and B in the low-frequency region below $10^3\ Hz$. As the frequency increases, the imaginary part of the impedance traces a semicircular path. The absolute value of the negative capacitance decreases with increasing frequency, passing through a minimum value and

eventually becoming positive capacitance. As $-1/\omega C$ approaches zero, C reaches its maximum value, corresponding to the peak of $\tau = R_s C_s$ in Figs. 6 (a) and 6 (b).

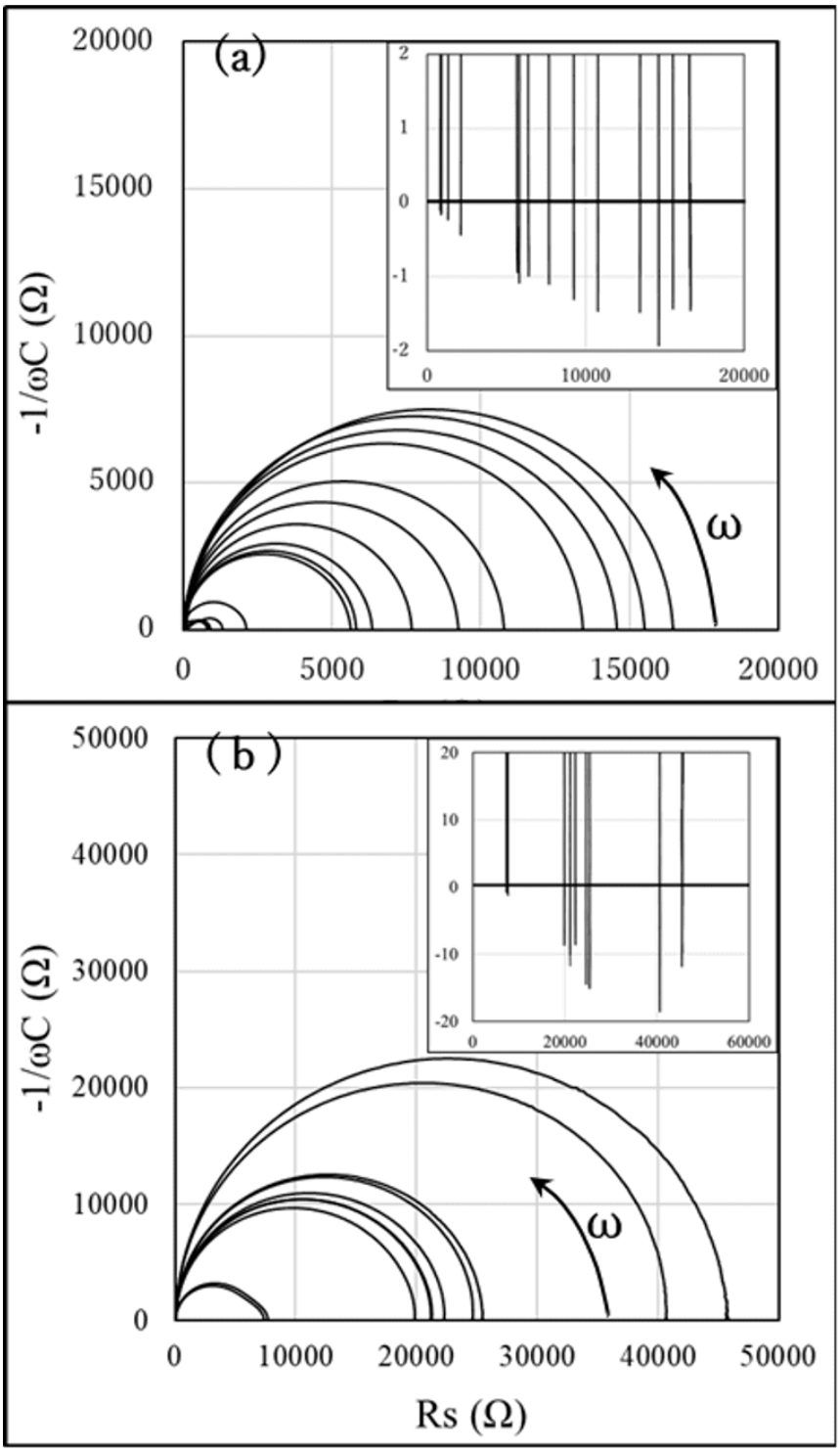

Figure 7. Cole–Cole plots for samples A (a) and B (b) at various .

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Based on these results, we now discuss the characteristics of negative capacitance. First, negative capacitance is only observed in the low-frequency region in the two-Si-resistor structure. A sufficient time is required for the change in charge Q due to the conduction current, polarization current, and tunneling current at low frequencies.

Second, negative capacitance is affected by the DC bias but is independent of the AC signal amplitude.

Third, controlling the distance between the two resistors allows for the interface capacitance to be varied between positive and negative values.

Fourth, the tunneling current plays a crucial role in the formation of negative capacitance. The tunneling current leaks charge Q and enables the condition $dQ/dV < 0$, contributing to the negative capacitance.

Fifth, contact resistance at the interface of the two-resistor structure accumulates charge Q and enables the condition $dQ/dV > 0$, contributing to positive capacitance.

Finally, the capacitance of the two-resistor structure is volatile. The conduction and tunneling currents only reach zero when the contact resistance becomes infinite, at which point charge accumulation due to the polarization current can be observed.

In conclusion, we fabricated an interface structure by angulation processing on the surface of a Si crystal, where two resistors contact each other. It became evident that the contact areas where conduction and polarization currents flow contribute to positive capacitance, while the non-contact areas where tunneling current flows contributes to negative capacitance. Furthermore, the negative capacitance effect holds promise for applications in two-dimensional inductor devices and integrated circuits without coils.

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Declarations

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