Review of: "The field-effect tunneling transistor nMOS, as an alternative to conventional CMOS by enabling the voltage supply (VDD) with ultra-low power consumption,"

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Potential competing interests: No potential competing interests to declare.

> *The field-effect tunneling transistor nMOS, as an alternative to conventional CMOS by enabling the voltage supply (VDD) with ultra-low power consumption, enables energy-efficient computing during the sub-threshold slope (SS) range. This type of device has a reverse-bias gate structure, which is usually called a tunnel field-effect transistor nMOS.*

For low-power applications, nMOS is considered. This device has less static leakage current than a MOSFET and is more resistant to SCEs. The most outstanding feature of nMOS is the capacity to produce a reverse subthreshold swing (SS) of less than the 60 mV/decade thermal limit (at 300 K), which is related to common reverse mode nMOSs. A pseudo-thermal SS is achievable because the drain current in nMOSs is generated by source-to-channel carrier injection, which is often under the band tunneling radius. It is placed in the quantum mechanical band (BTBT).

> *Transistor speed nMOS is proportional to the current. The higher the current, the faster the transistor will be able to amplify and charge (the sequential capacitor voltage). For a given transistor speed and maximum acceptable subthreshold leakage, the subthreshold slope thus defines a minimum threshold voltage. Decreasing the threshold voltage is an essential part of the idea to scale the constant amount of nMOS to overcome some challenges associated with the nMOS structure, such as its need for ultra-sharp doping profiles; however, such devices may suffer from gate leakage due to the presence of large vertical fields in the nMOS transistor structure.*

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